**Digital Design and Computer Organization Laboratory**

**3rd Semester, Academic Year 2024**

Date: 17/10/2024

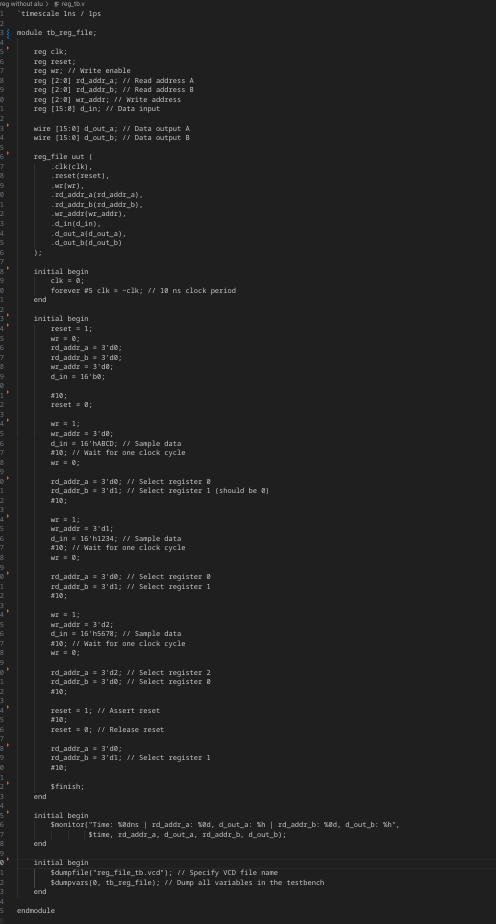
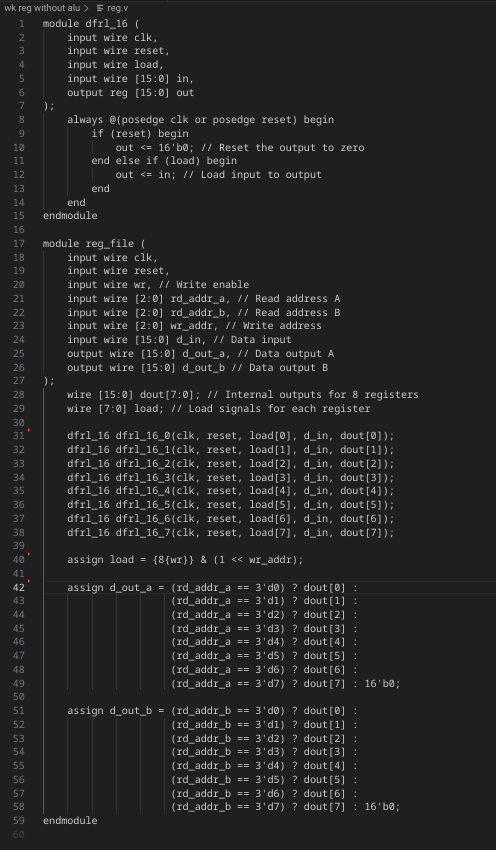
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| Name: Rithvik Rajesh Matta | SRN: PES2UG23CS485 | Section: H |

Week#\_\_\_\_9\_\_\_\_\_\_\_ Program Number: \_\_\_\_9\_\_

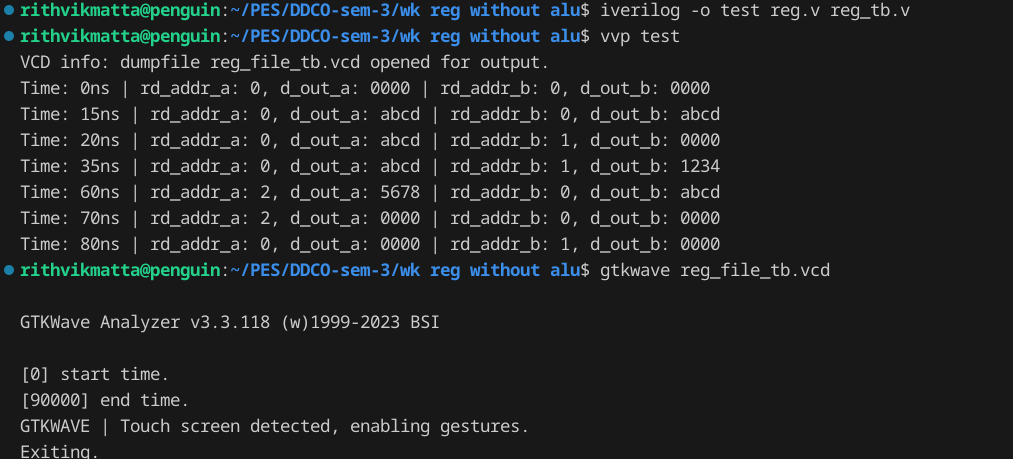
Aim of the Experiment:

CONSTRUCT A REGISTER FILE (without alu), FROM WHICH TWO 16-BIT VALUES CAN BE READ, AND TO WHICH ONE 16-BIT VALUE WRITTEN, EVERY CLOCK CYCLE.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code Screenshot



II. Verilog VVP Output Screen Shot



III. GTKWAVE Screenshot



IV. Output Table (Truth Table)

|  |  |  |  |
| --- | --- | --- | --- |
| rd\_addr\_a | d\_out\_a | rd\_addr\_b | d\_out\_b |
| 0 | 0000 | 0 | 0000 |
| 0 | abcd | 0 | abcd |
| 0 | abcd | 1 | 0000 |
| 0 | abcd | 1 | 1234 |
| 2 | 5678 | 0 | abcd |
| 2 | 0000 | 0 | 0000 |
| 0 | 0000 | 1 | 0000 |

If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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